

Fig. 1A SEM photograph (cross section)

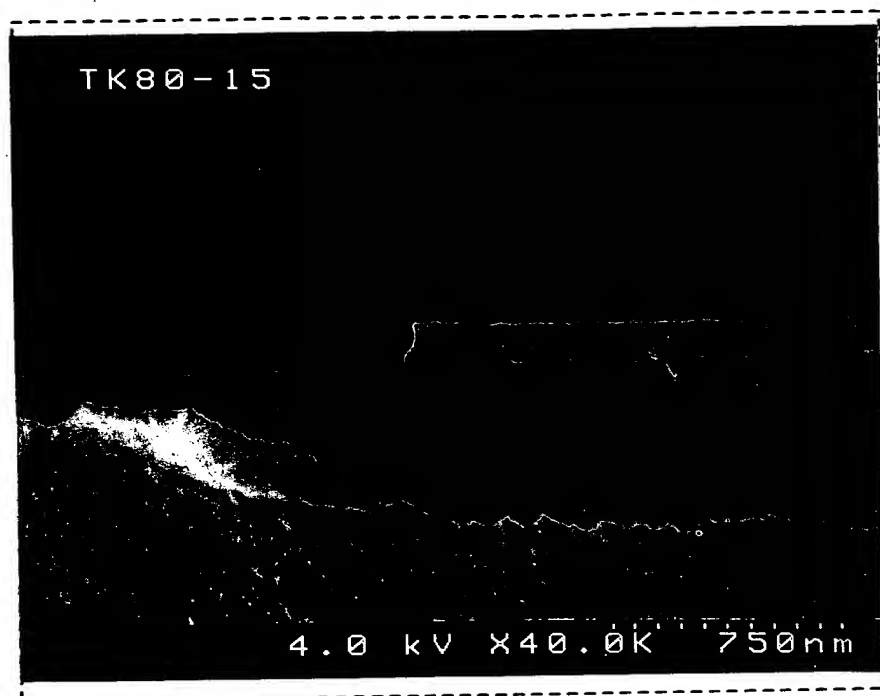


Fig. 1B schematic diagram of enlarged electrode edge portion

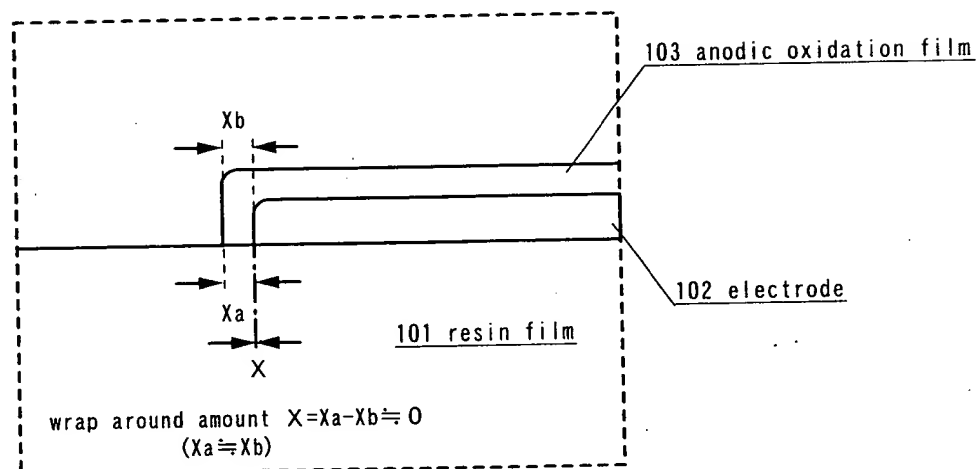


Fig. 2

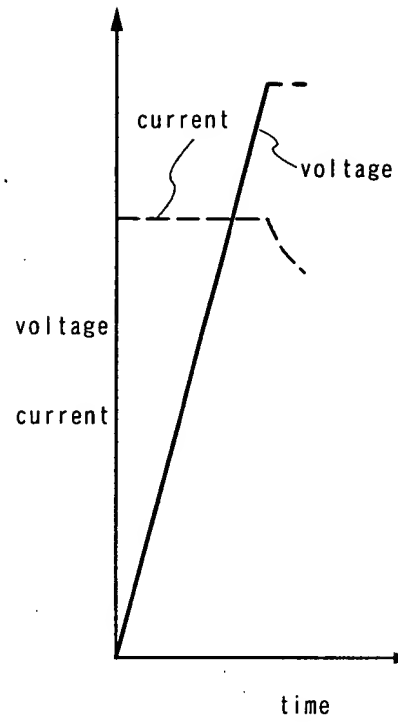


Fig. 3A

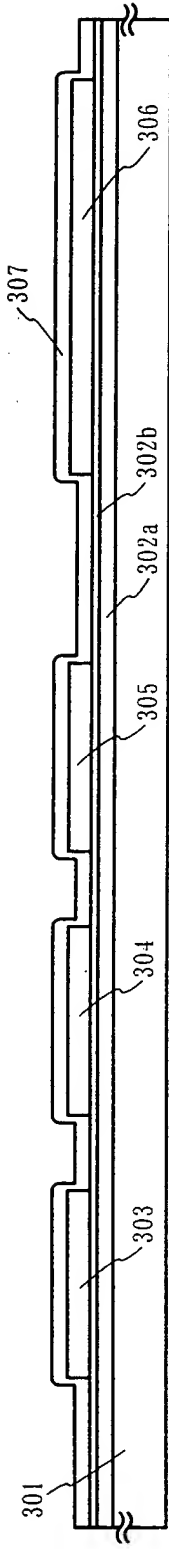


Fig. 3B

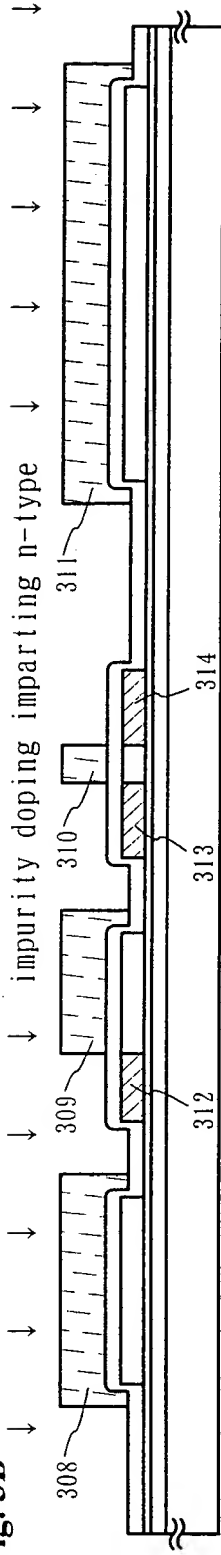


Fig. 3C

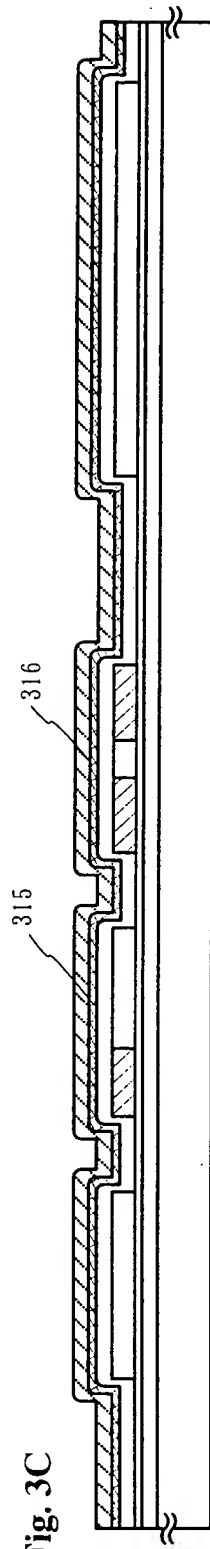


Fig. 3D

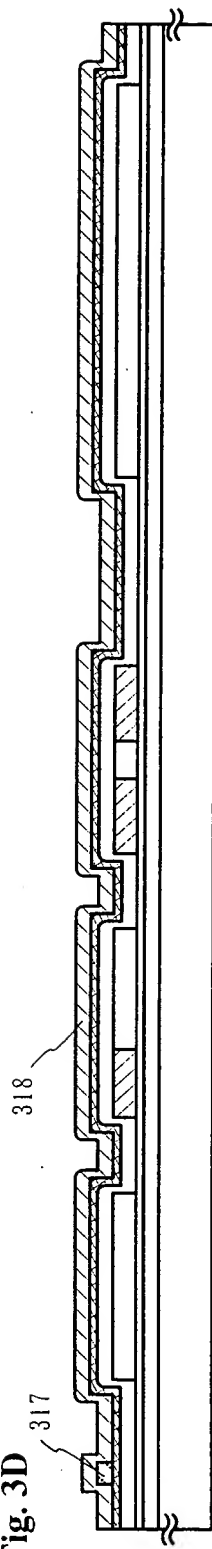


Fig. 4A

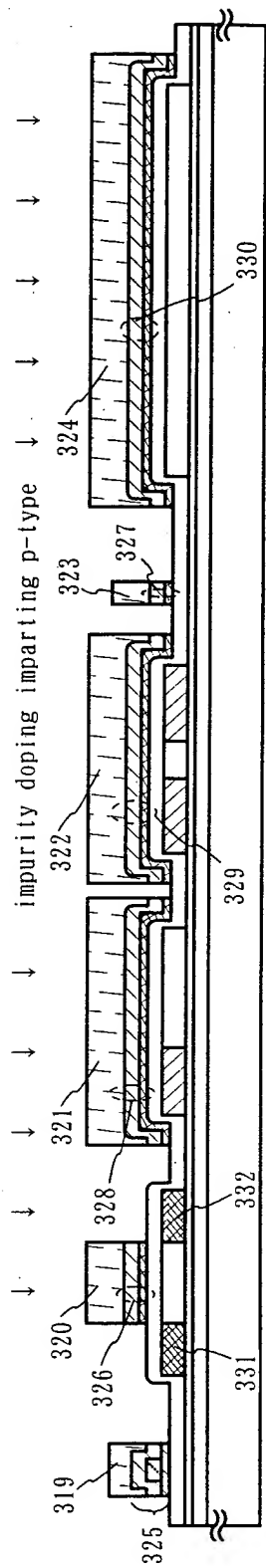


Fig. 4B

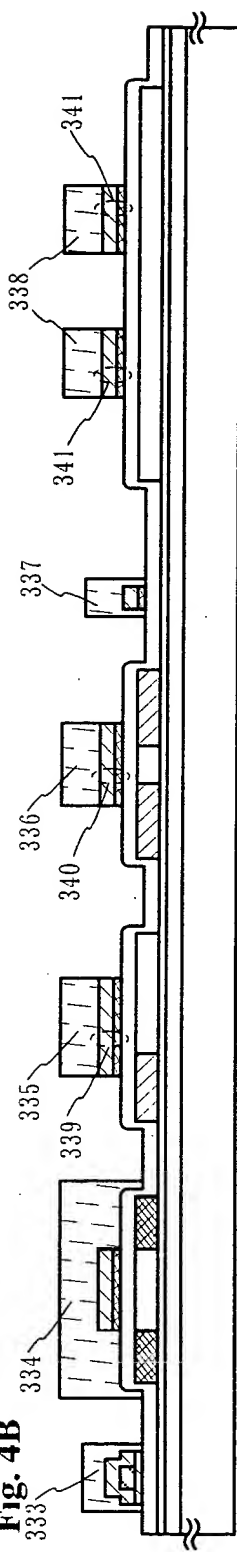


Fig. 4C

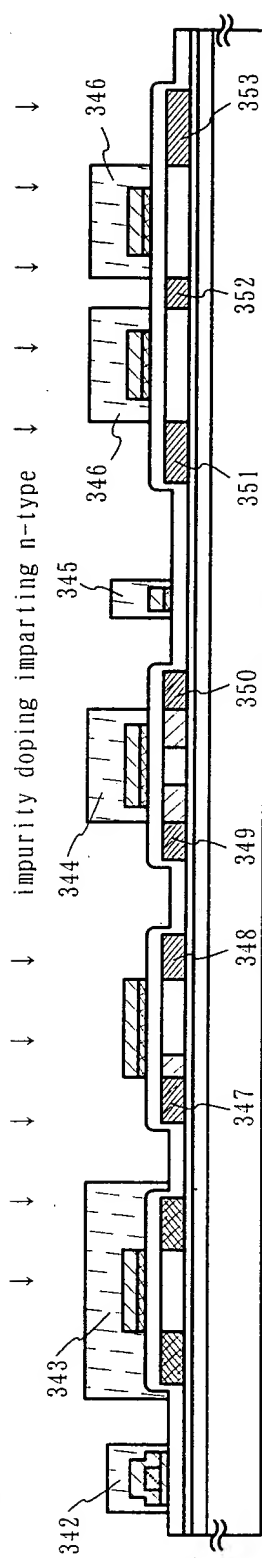


Fig. 5A

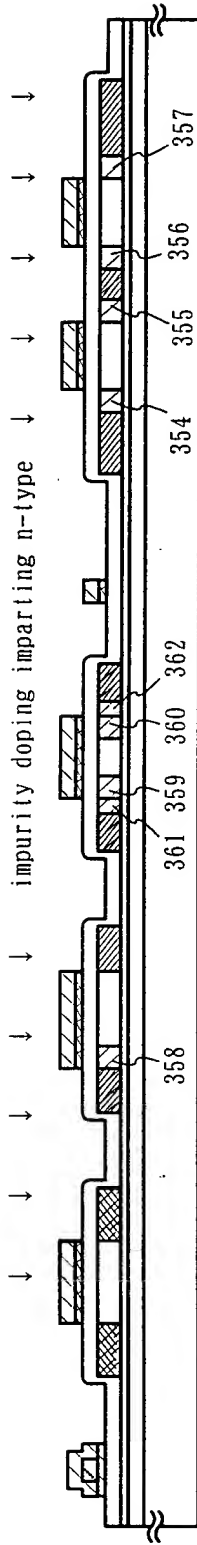


Fig. 5B

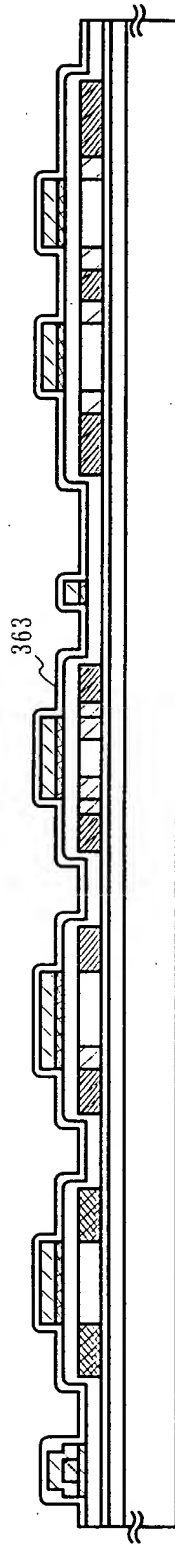


Fig. 5C

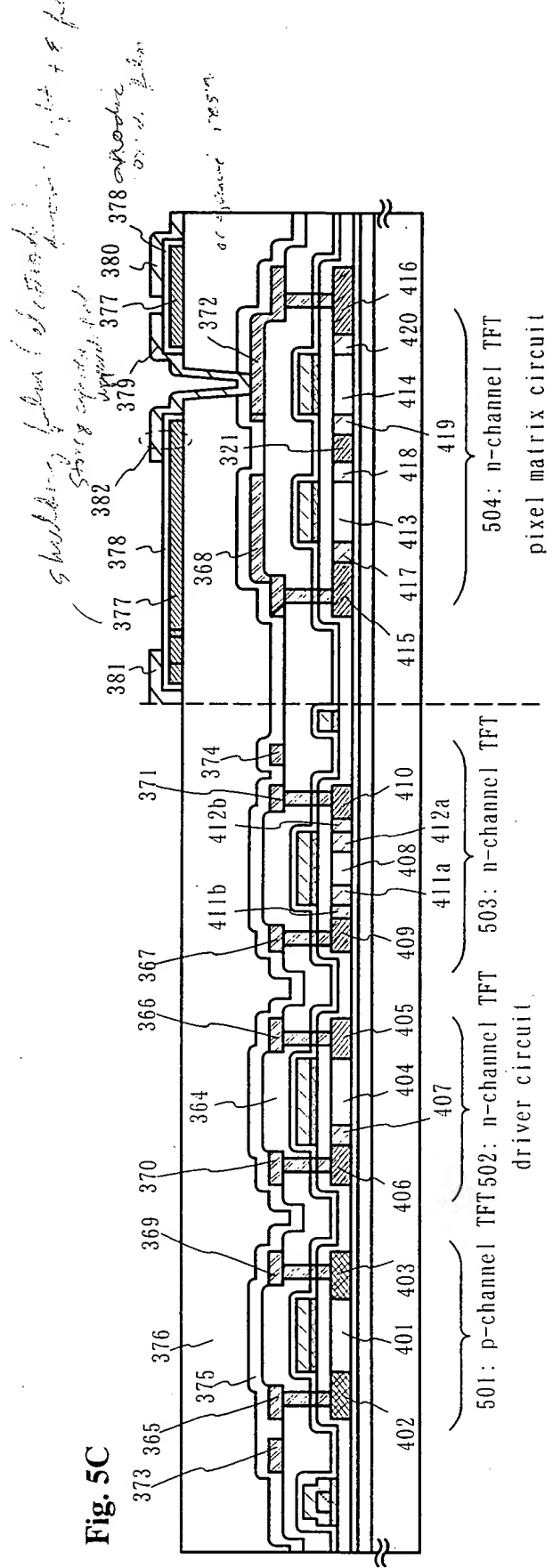


Fig. 6

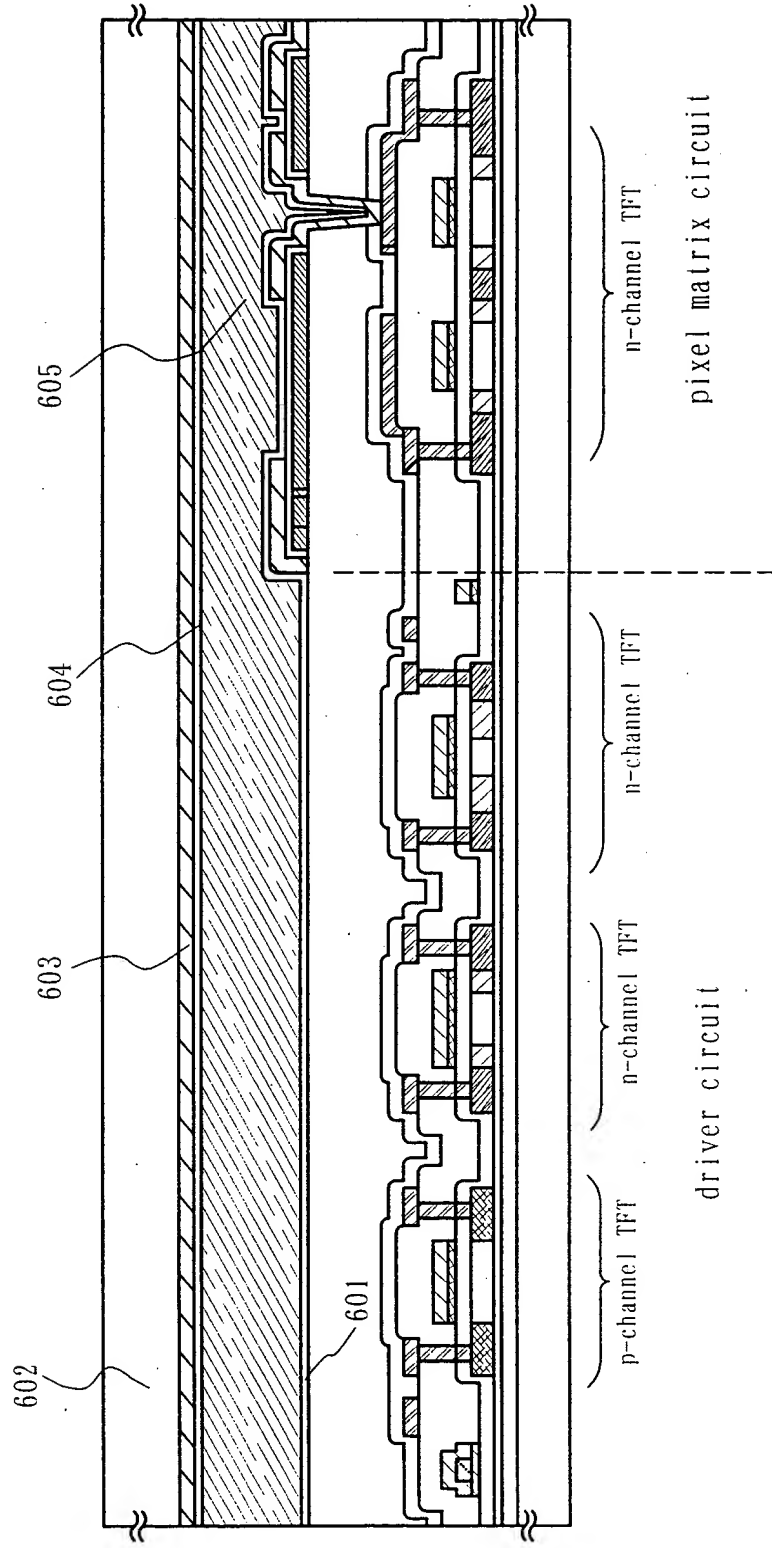


Fig. 7

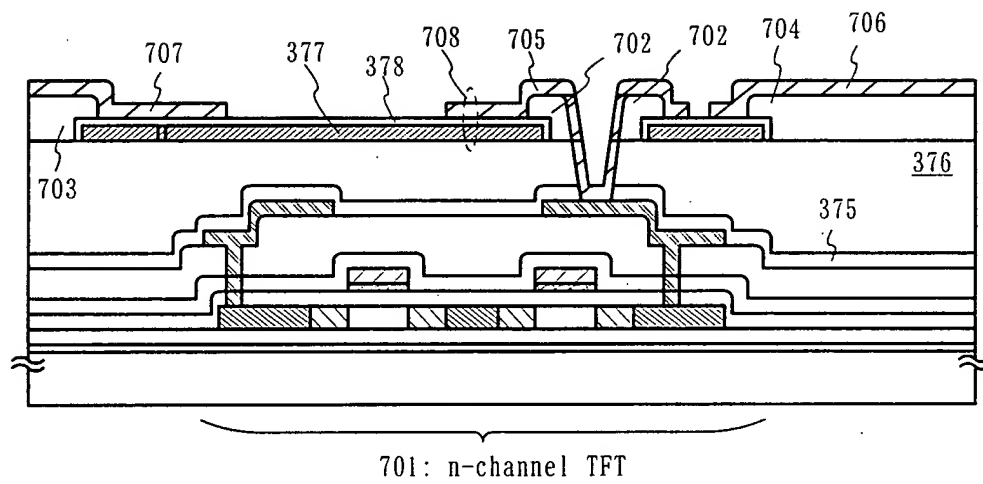


Fig. 8A

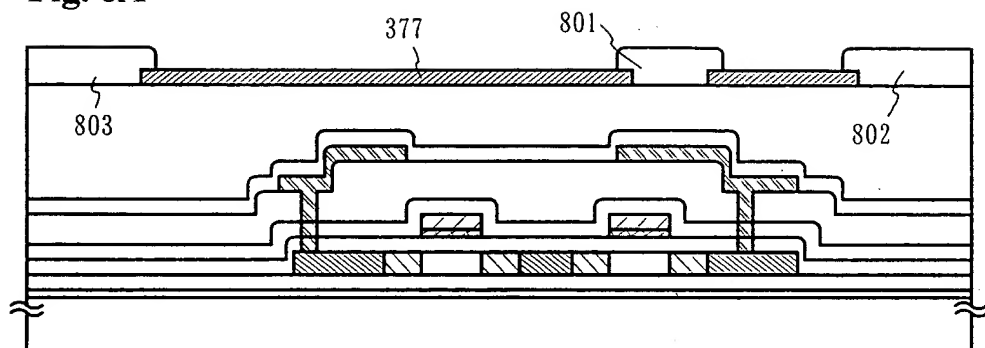


Fig. 8B

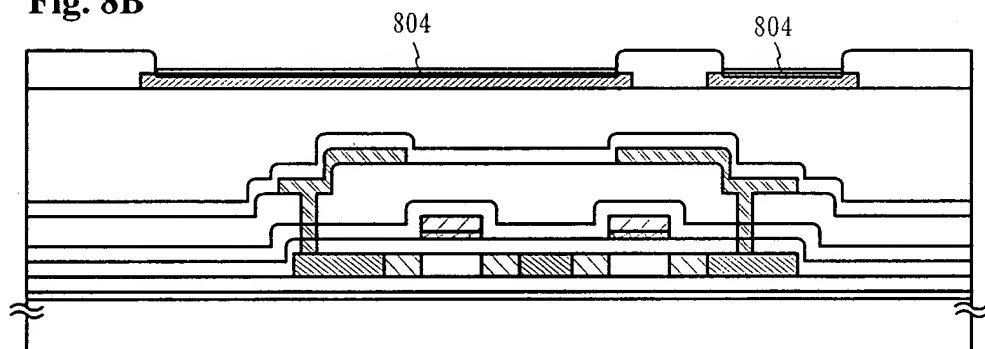


Fig. 8C

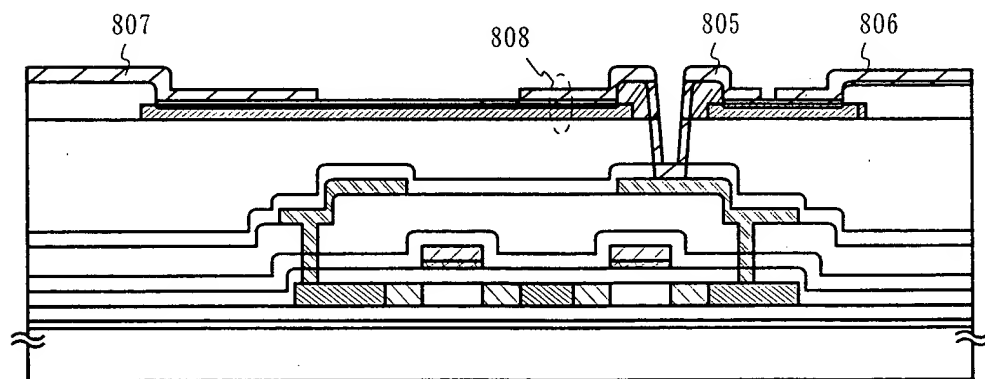


Fig. 9A

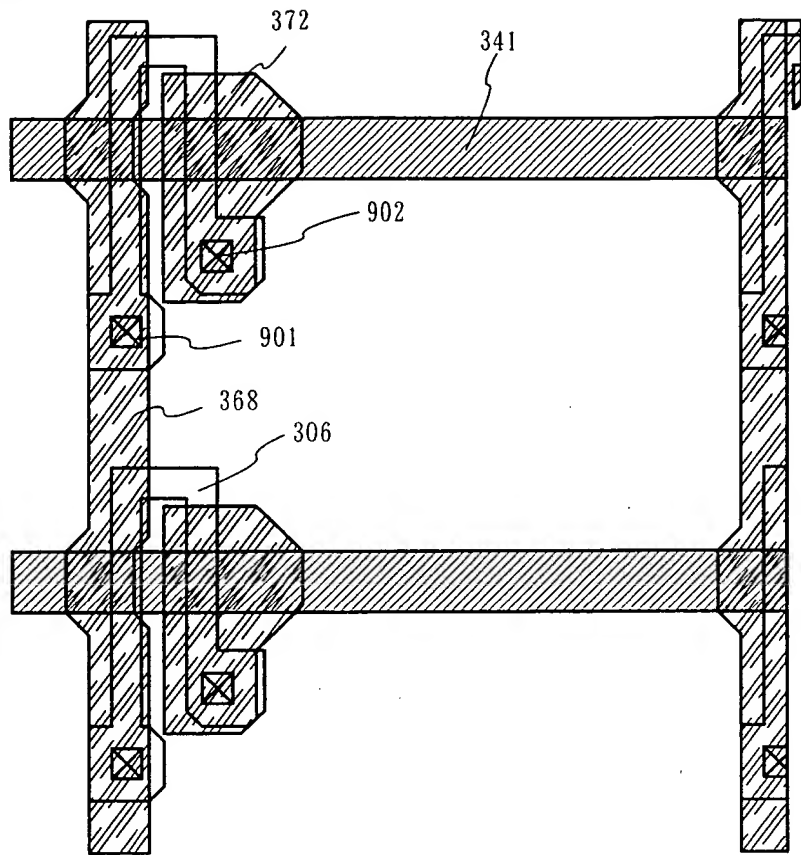


Fig. 9B

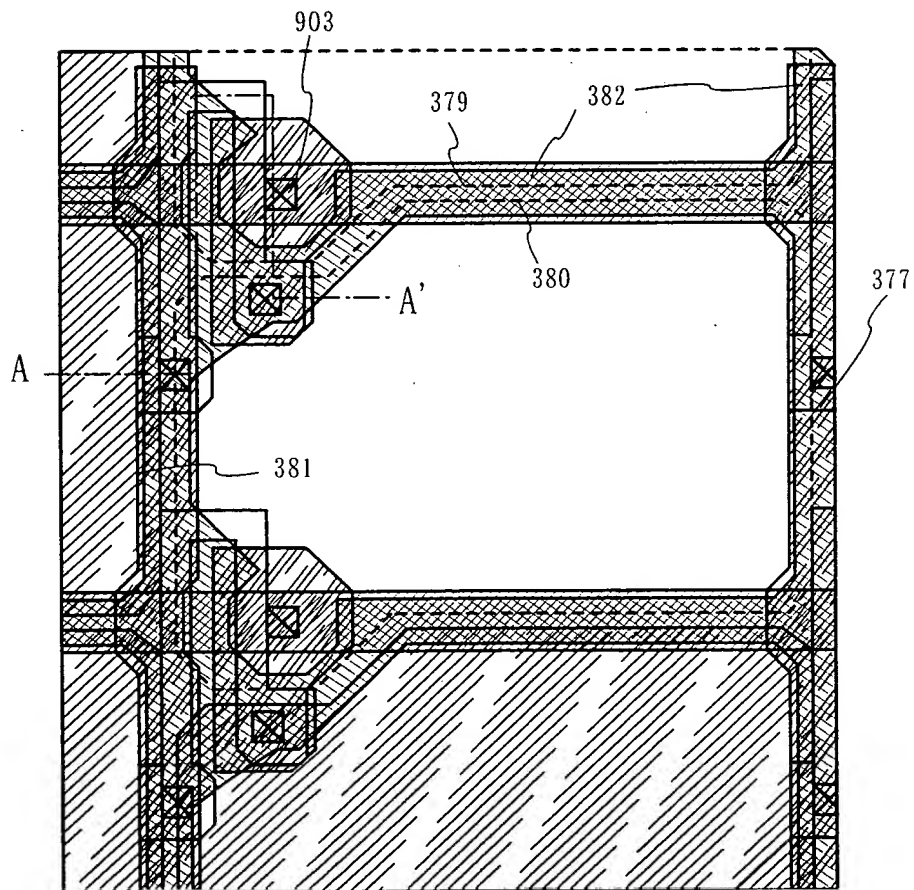


Fig. 10A

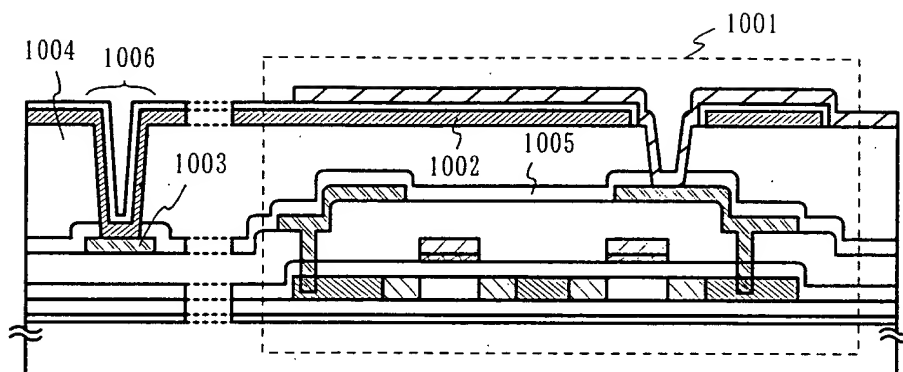


Fig. 10B

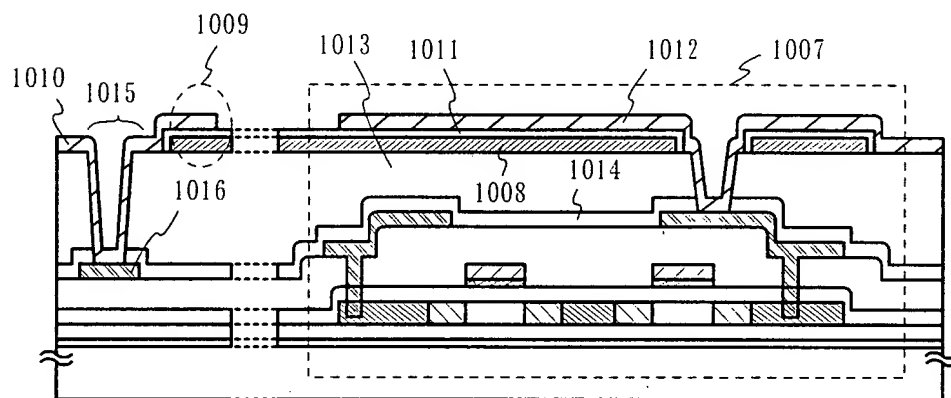


Fig. 11A

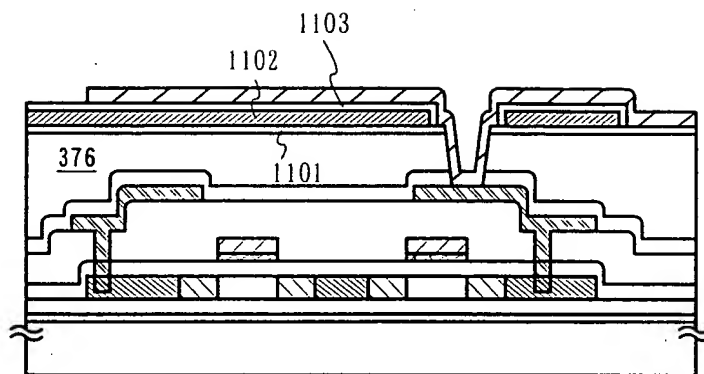


Fig. 11B

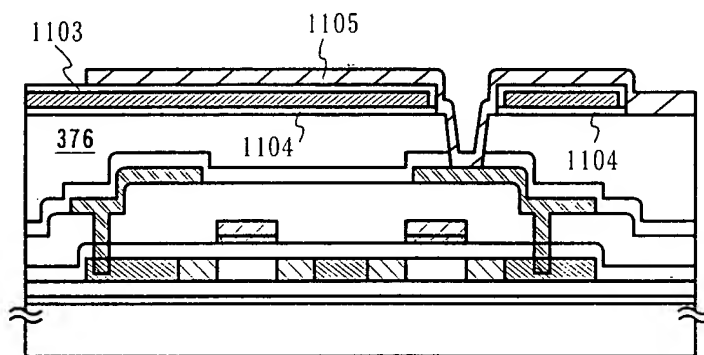


Fig. 12

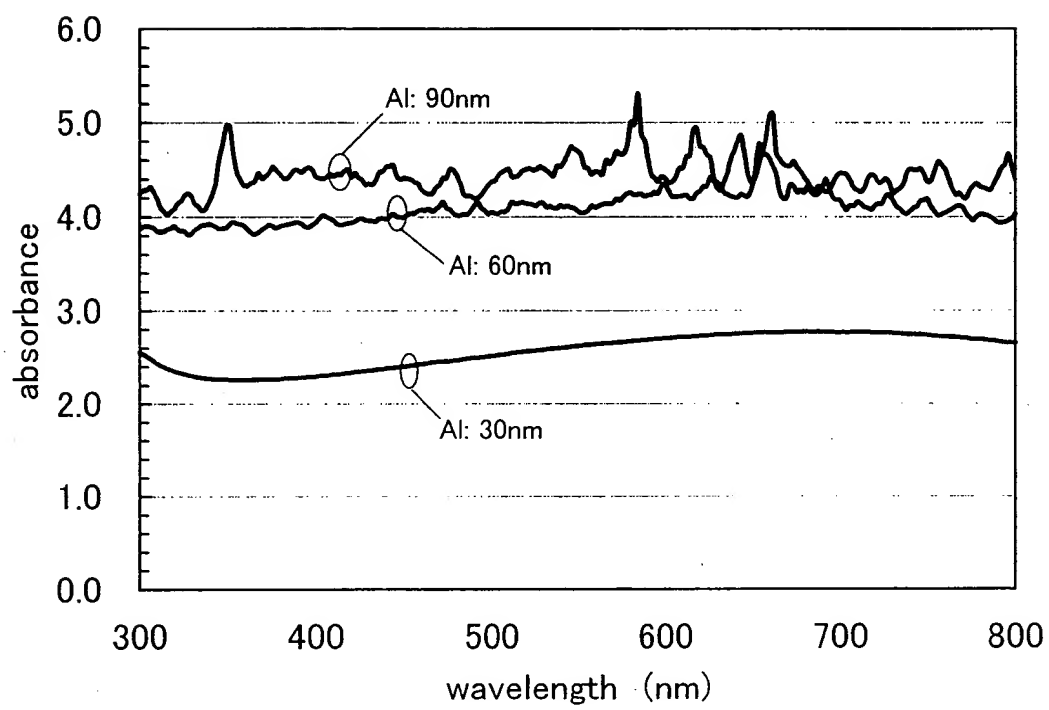


Fig. 13

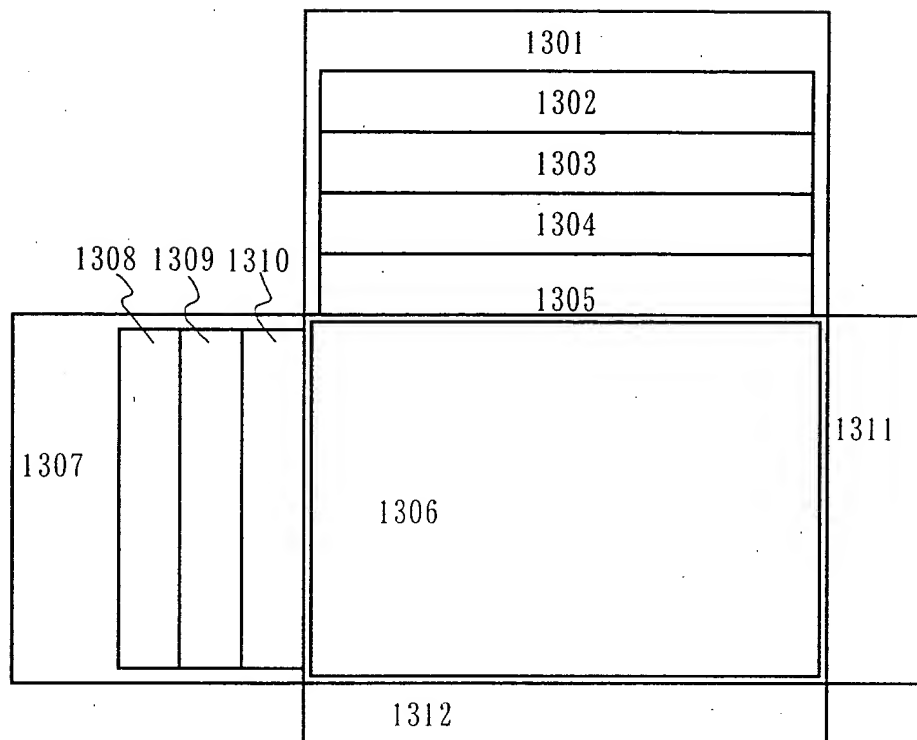


Fig. 14

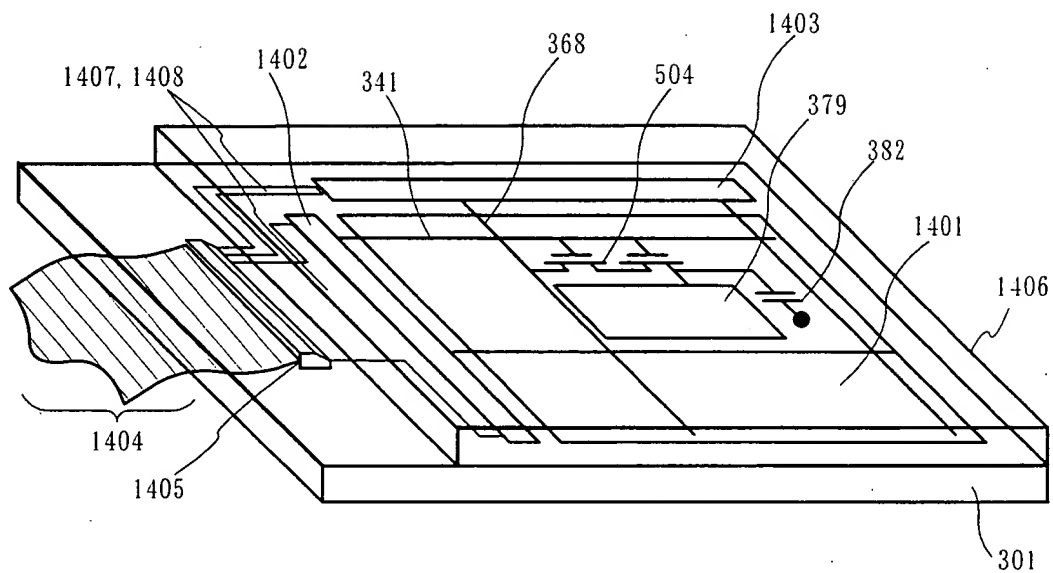


Fig. 15A

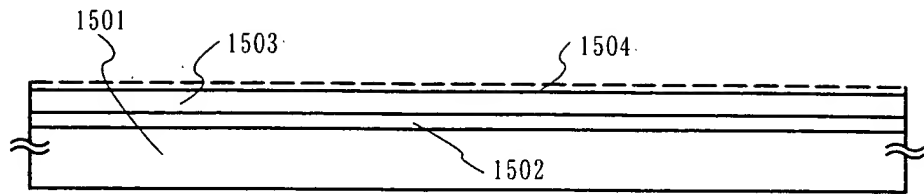


Fig. 15B

crystallization

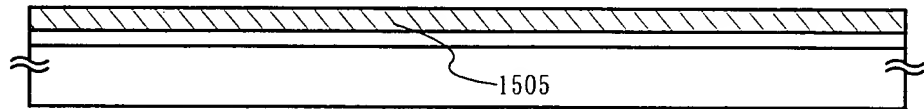


Fig. 15C

phosphorus dope

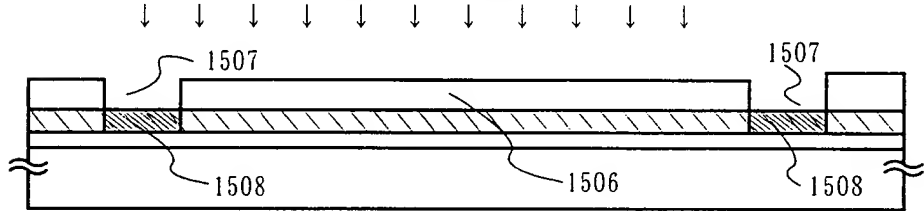


Fig. 15D

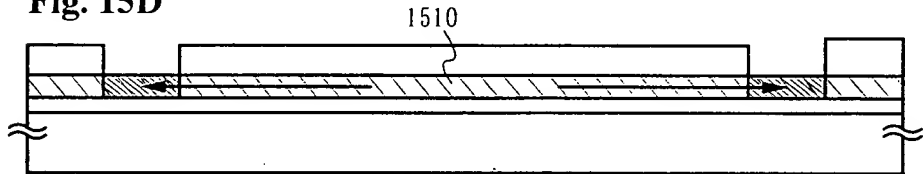


Fig. 15E

formation of active layer

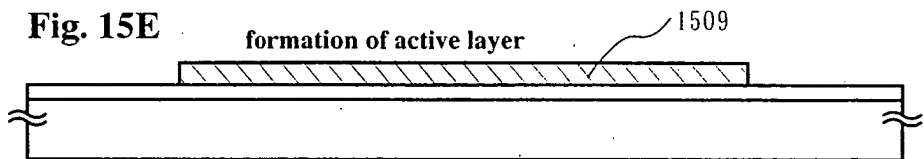


Fig. 16A

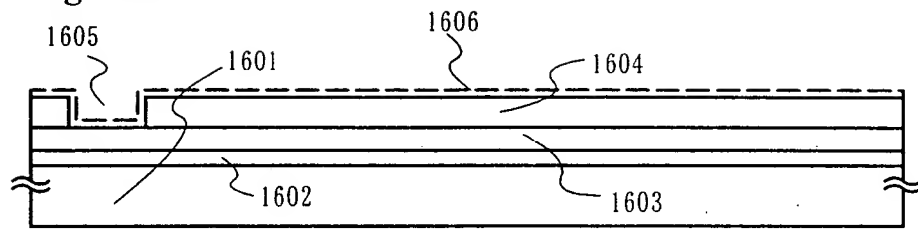


Fig. 16B

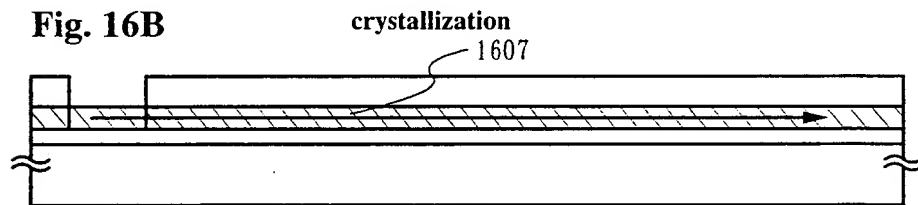


Fig. 16C

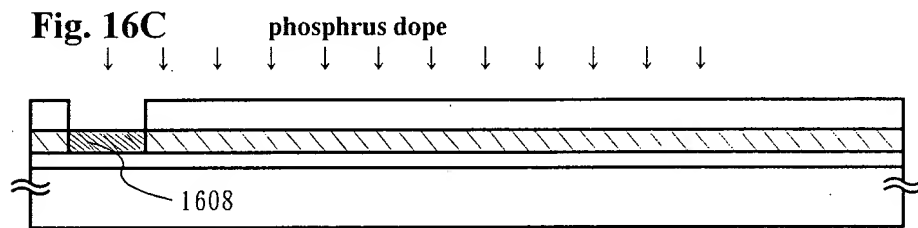


Fig. 16D

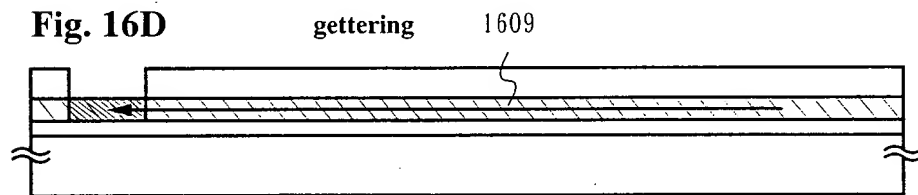


Fig. 16E

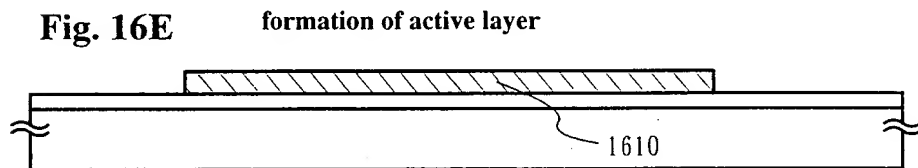


Fig. 17A

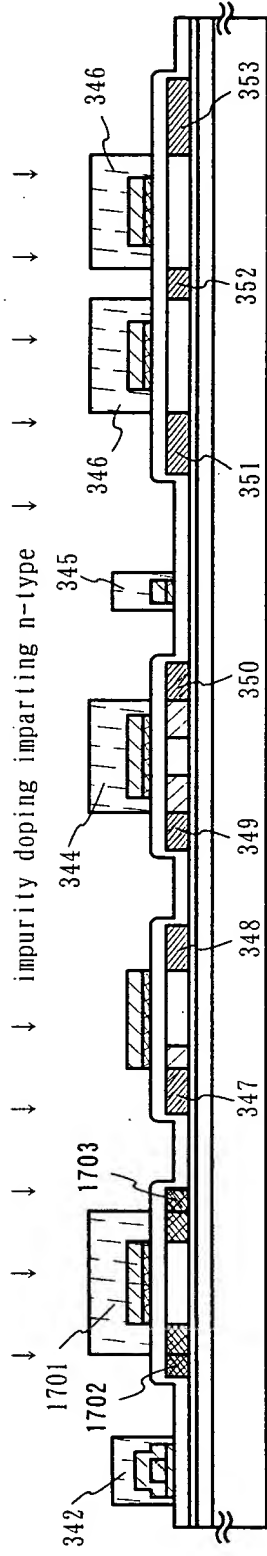


Fig. 17B

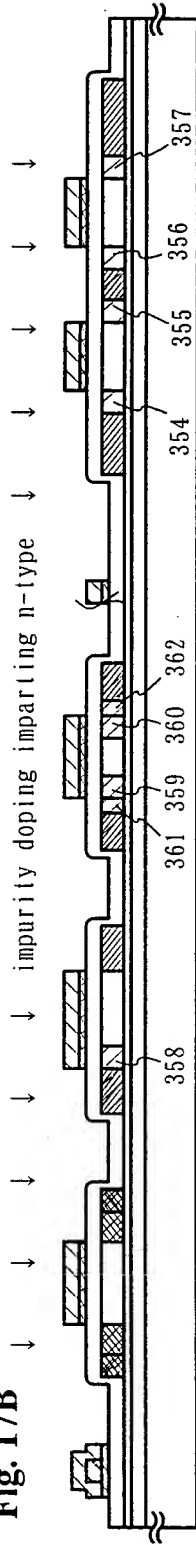


Fig. 17C

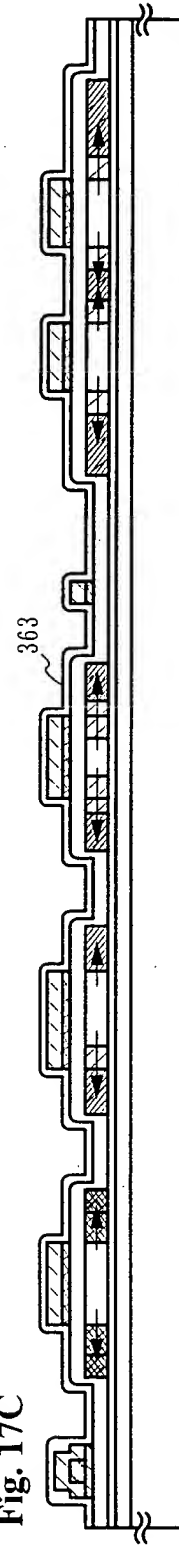


Fig. 18A

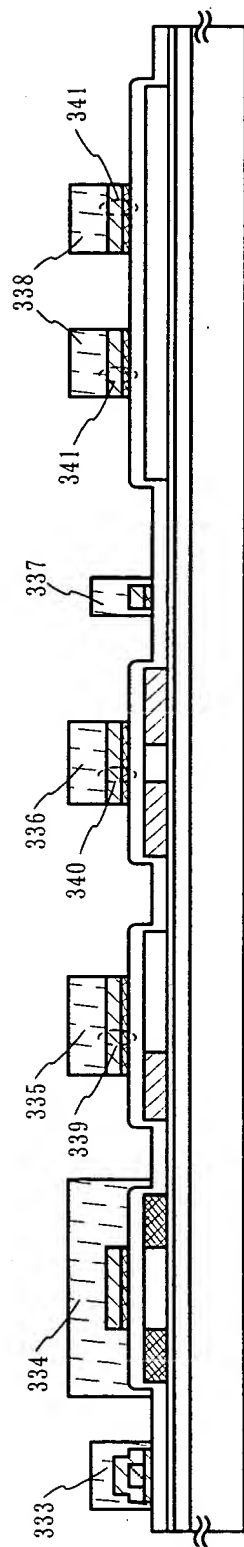


Fig. 18B forming n-- region

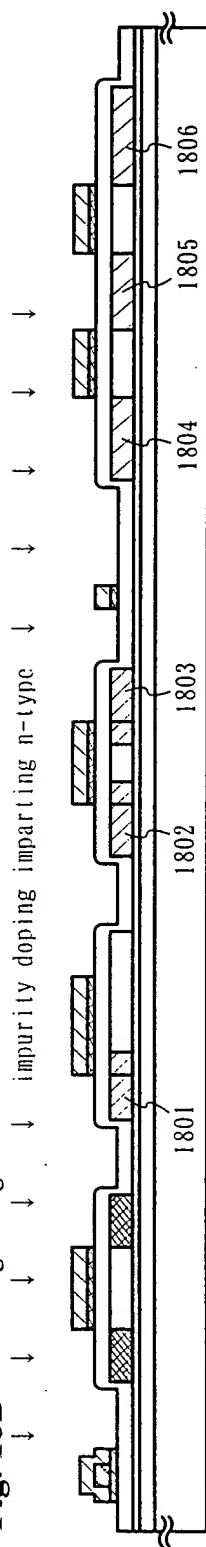


Fig. 18C forming n+ region

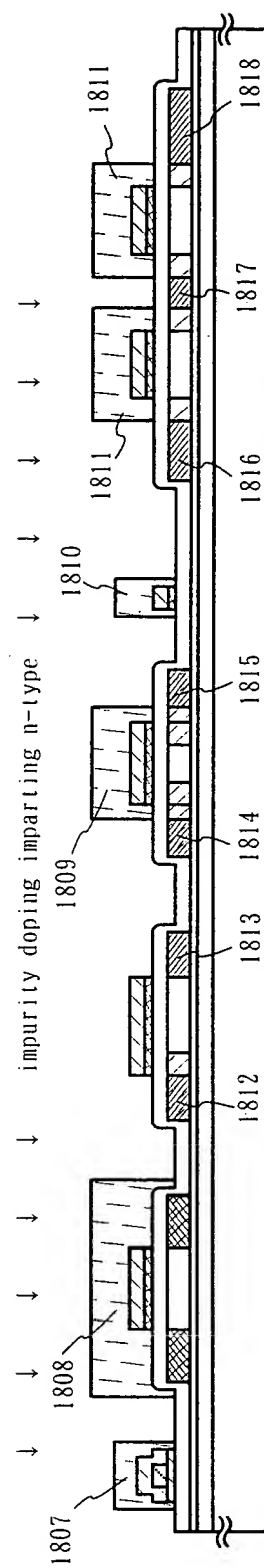


Fig. 19A forming n+ region

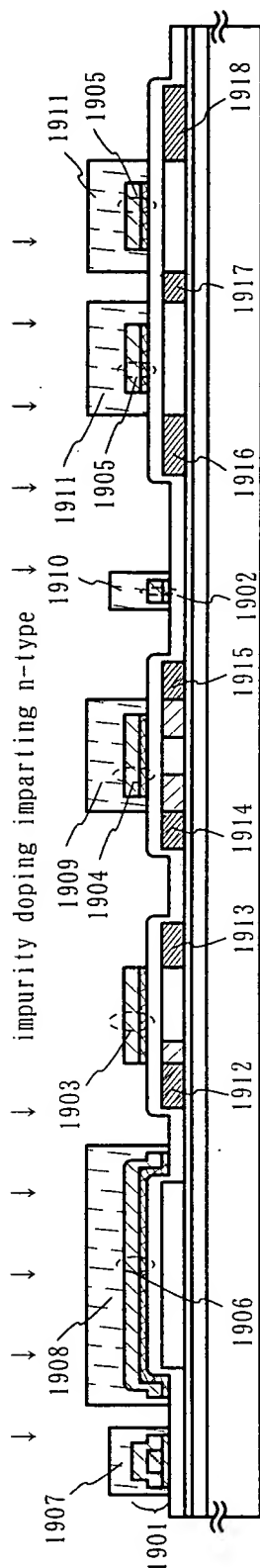


Fig. 19B forming p-ch TFT gate wiring, forming p++ region

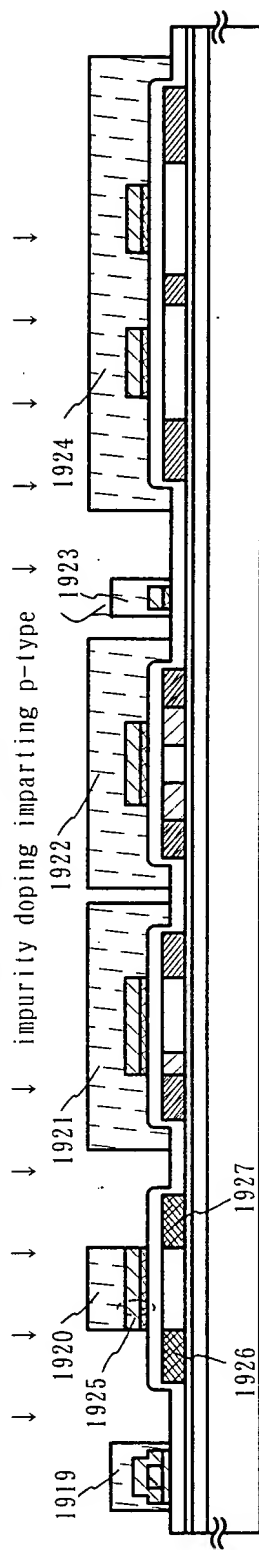


Fig. 19C forming n-- region

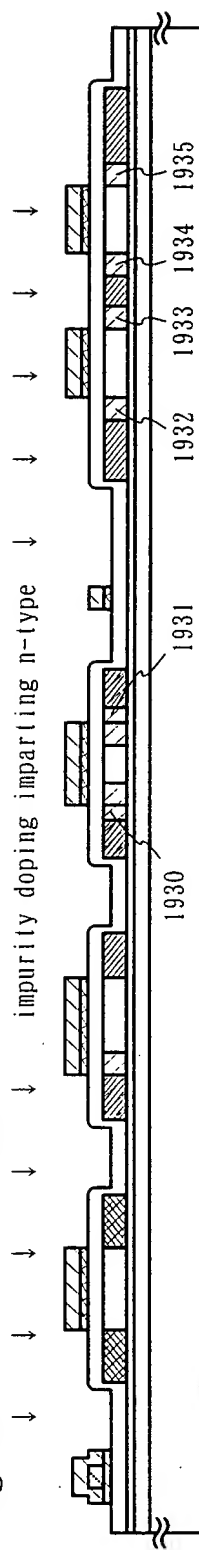


Fig. 20A forming n+ region

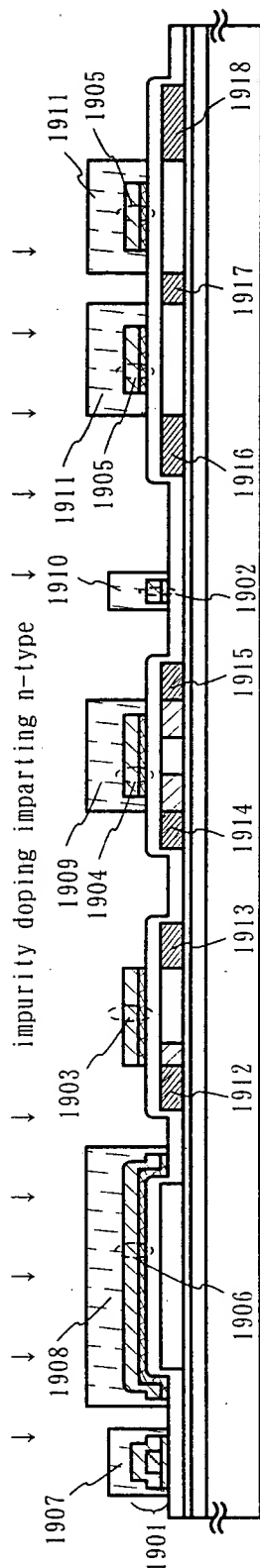


Fig. 20B forming n-- region

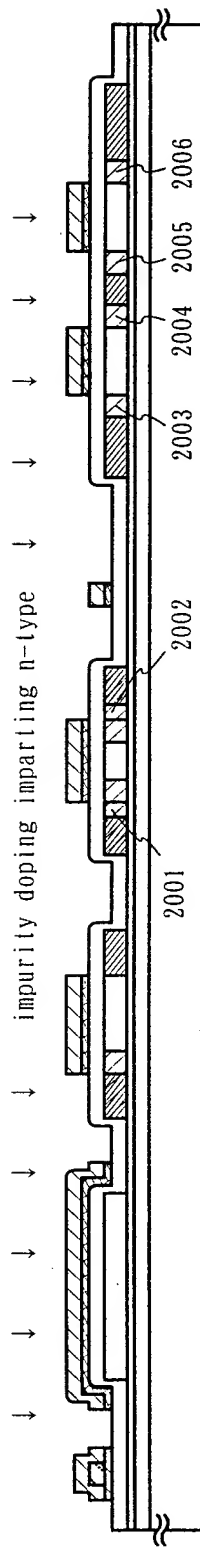


Fig. 20C forming p-ch TFT gate wiring, forming p+++ region

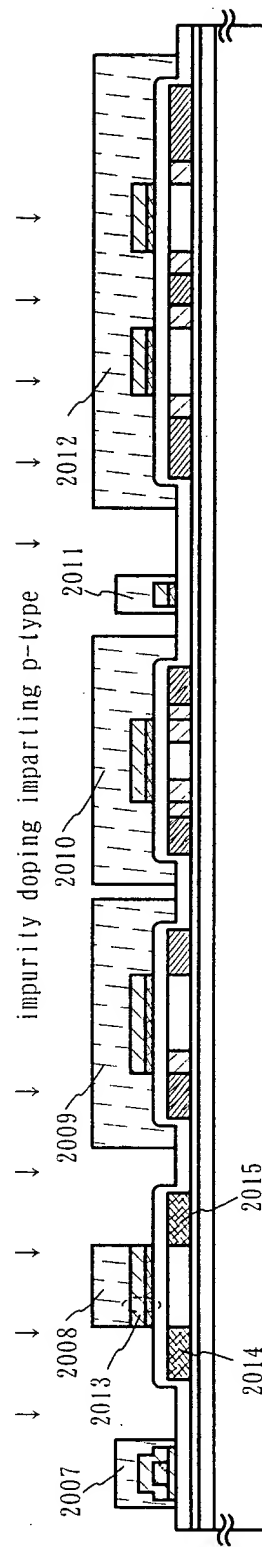


Fig. 21A forming n-ch TFT gate wiring

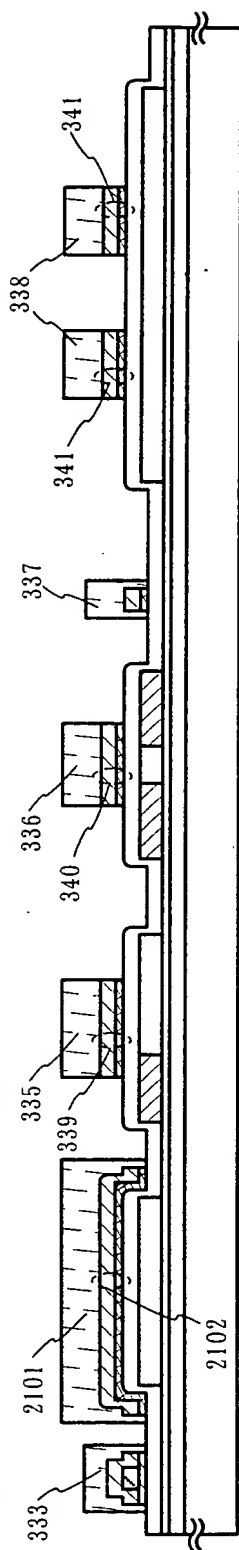


Fig. 21B forming n-- region

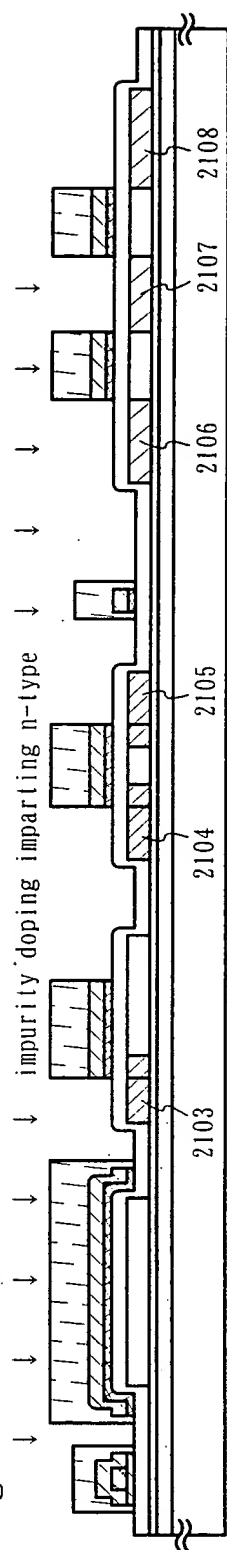


Fig. 21C forming n+ region

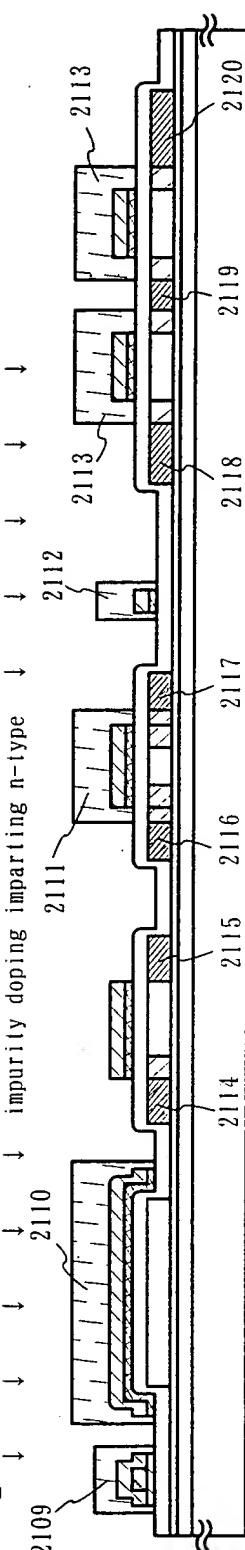


Fig. 21D forming p-ch TFT gate wiring, forming p++ region

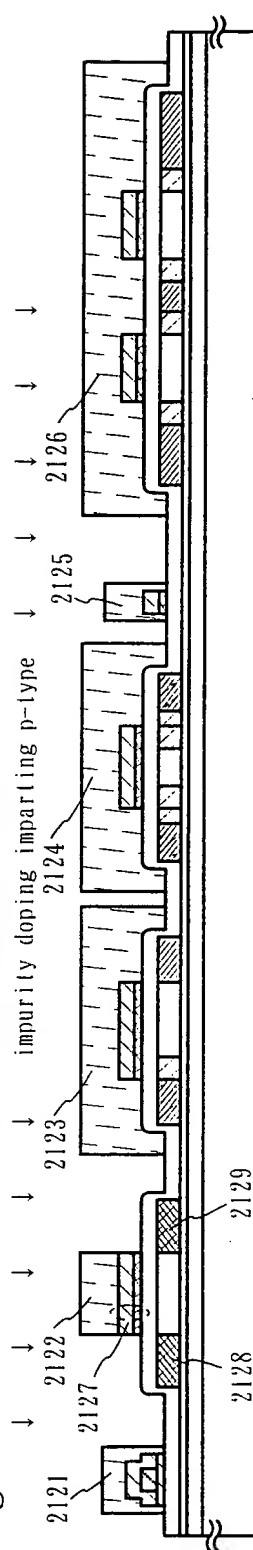


Fig. 22A forming n-- region

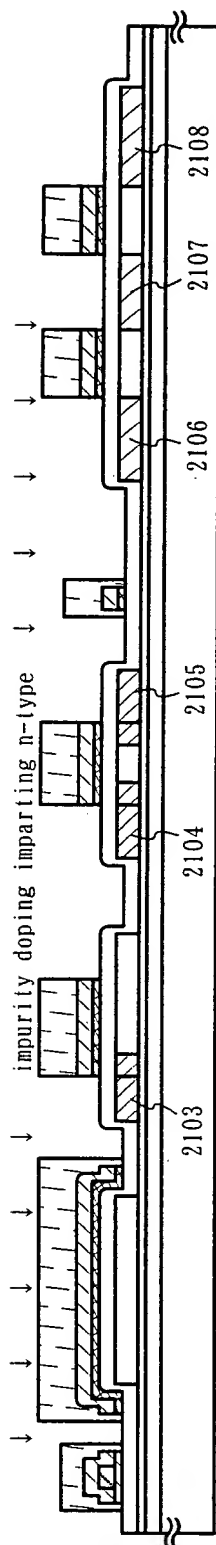


Fig. 22B forming p-ch TFT gate wiring, forming p++ region

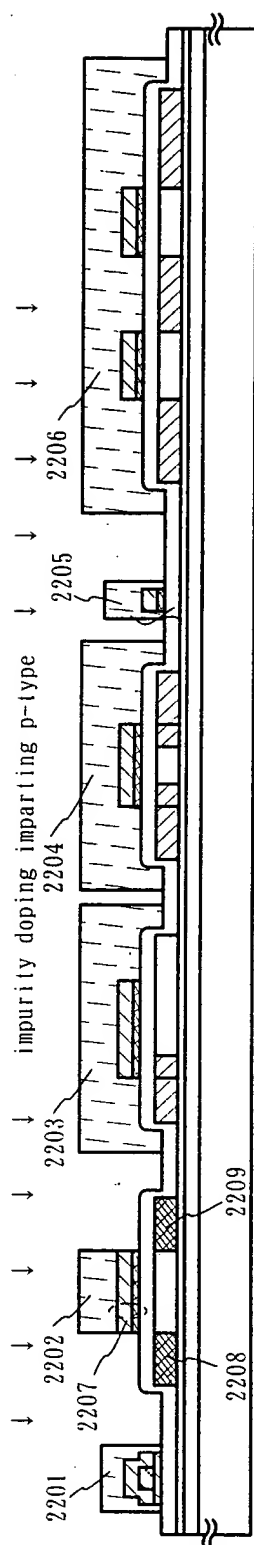


Fig. 22C forming n+ region

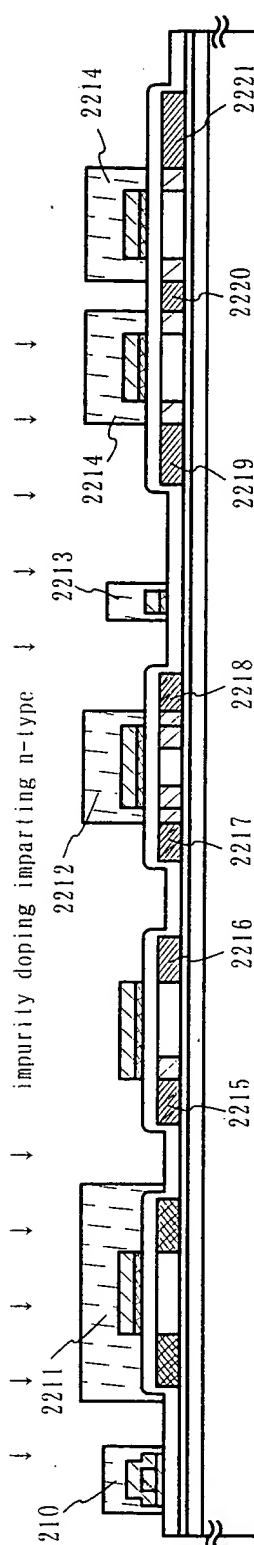


Fig. 23

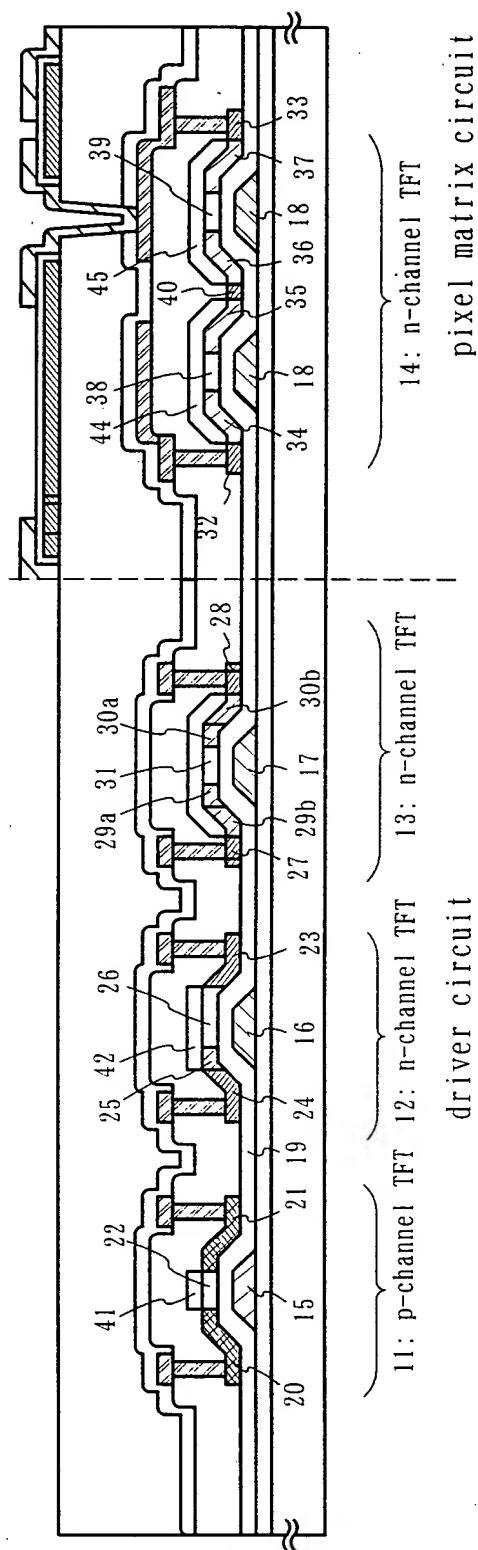


Fig. 24A

EL panel circuit diagram

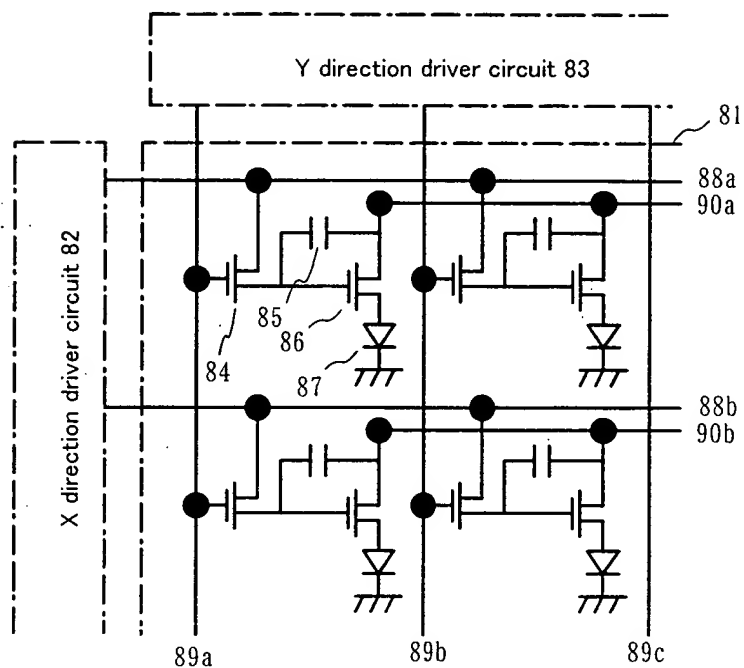


Fig. 24B

top view of EL panel pixel section

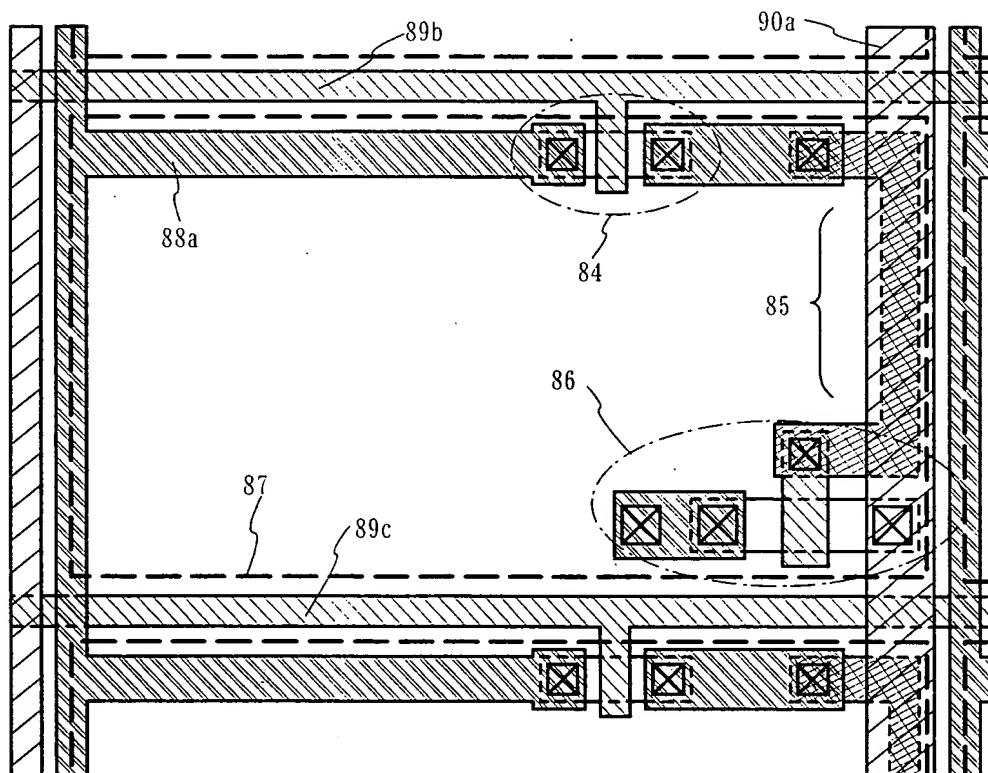


Fig. 25A

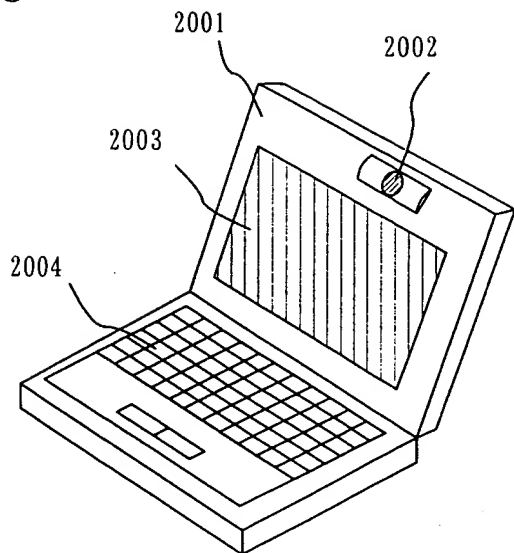


Fig. 25B

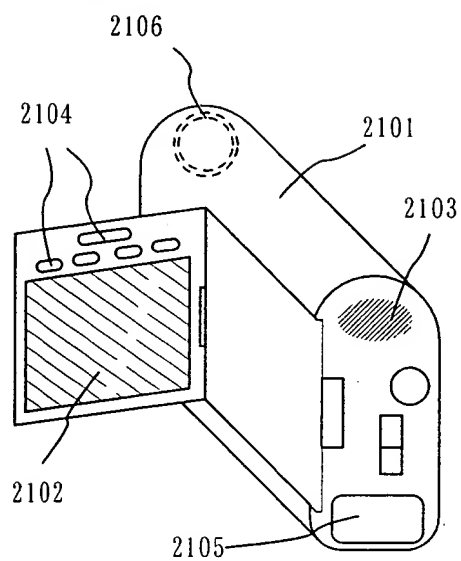


Fig. 25C

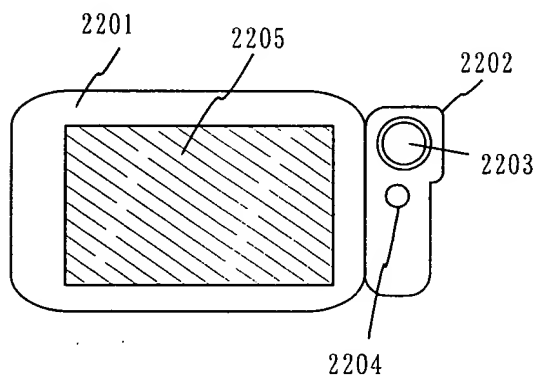


Fig. 25D

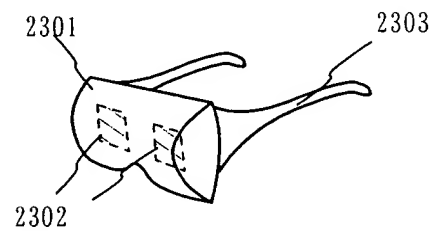


Fig. 25E

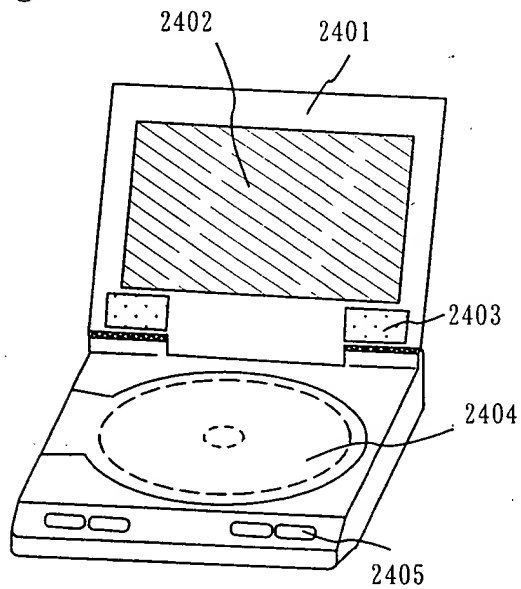


Fig. 25F

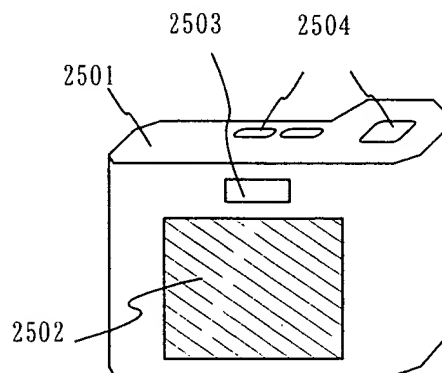


Fig. 26 **Prior Art**

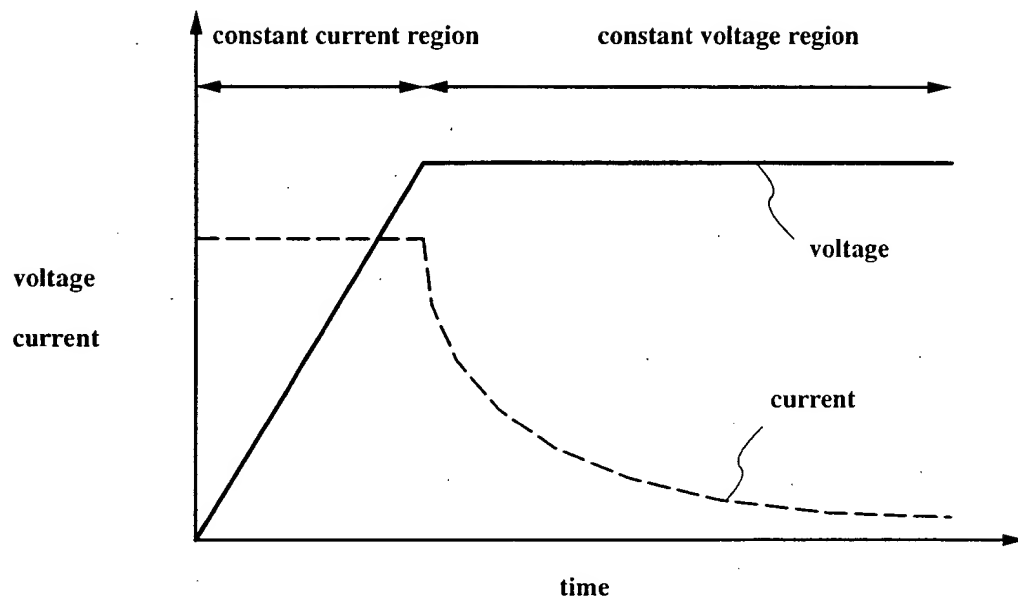


diagram showing the relationship between voltage and electric current between the electrodes in a conventional anodic oxidation process

Fig. 27A SEM photograph (cross section)

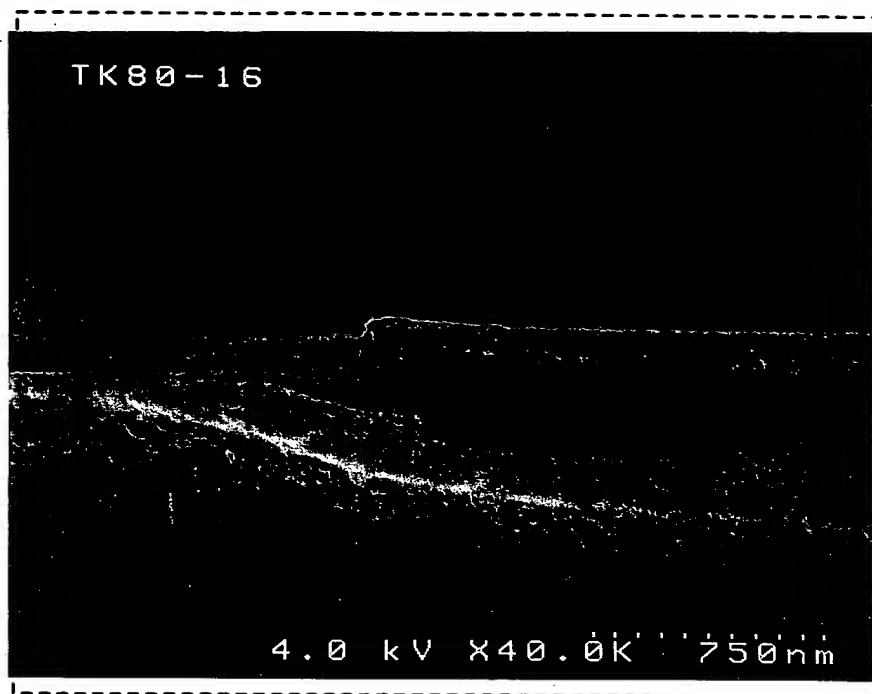
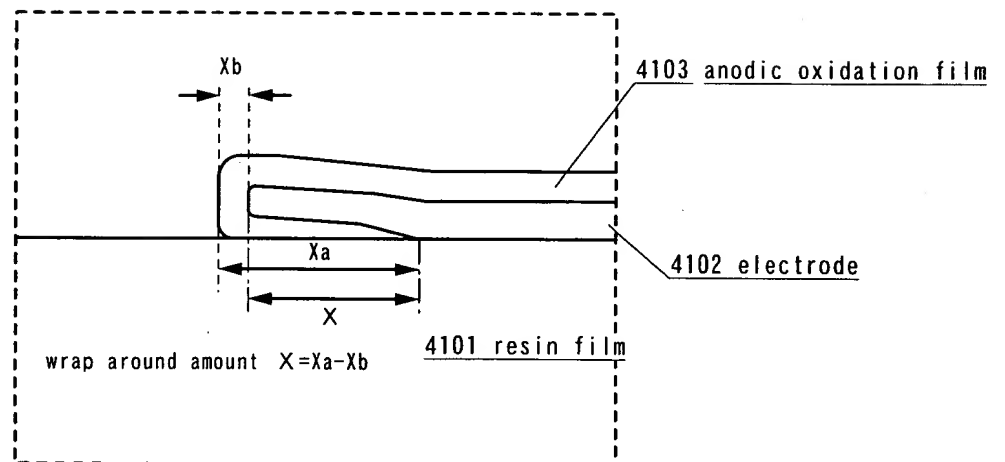


Fig. 27B schematic diagram of enlarged electrode edge portion



Prior Art

Fig. 28A

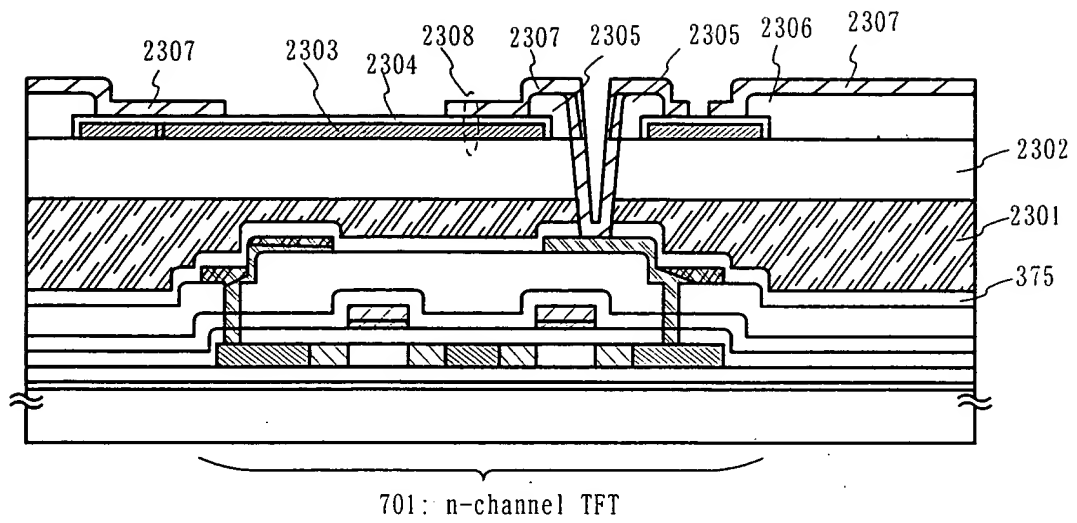


Fig. 28B

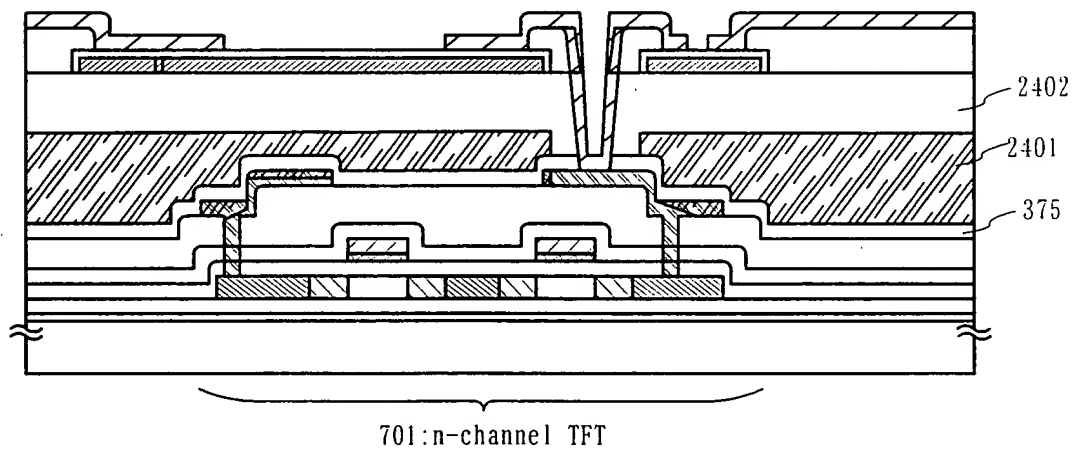


Fig. 29A

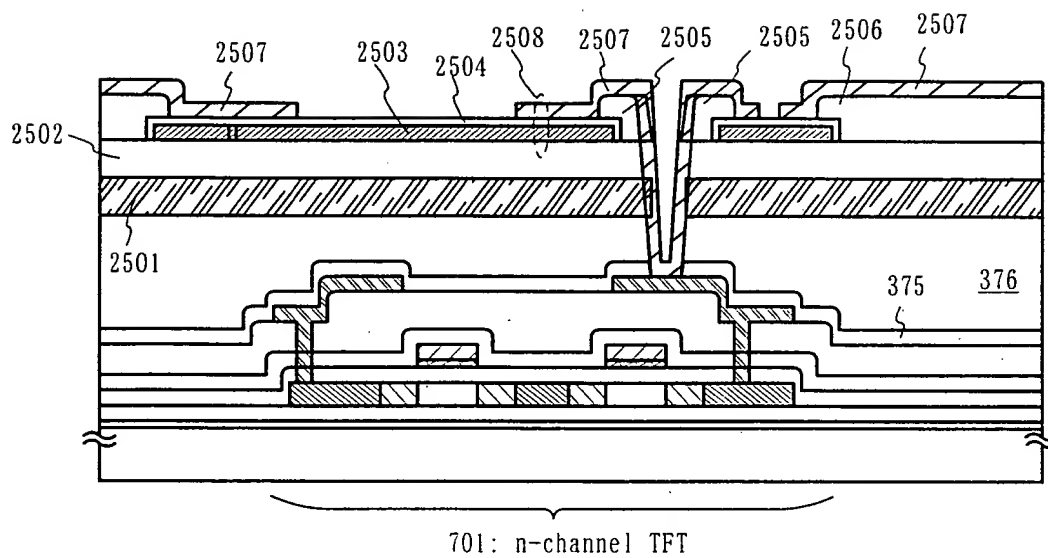


Fig. 29B

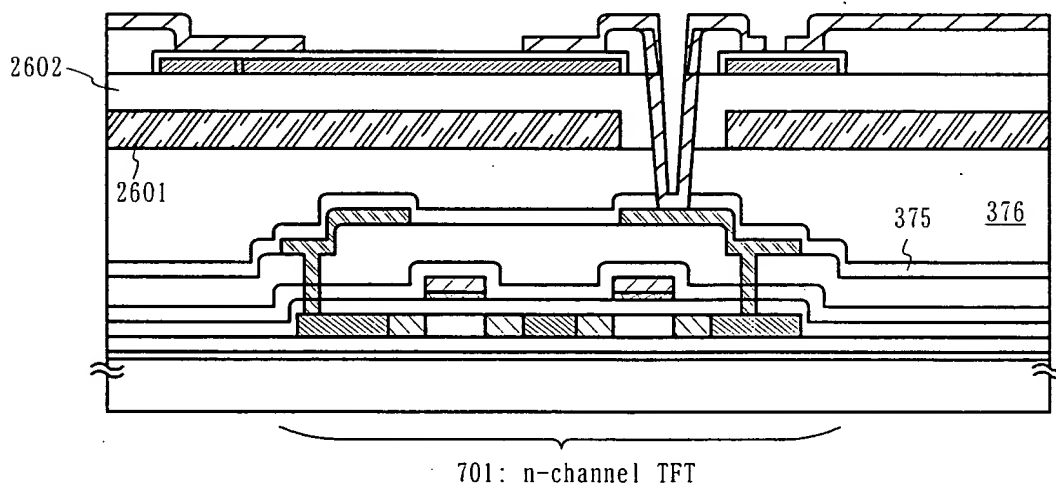


Fig. 30A

SEM photograph (cross section)

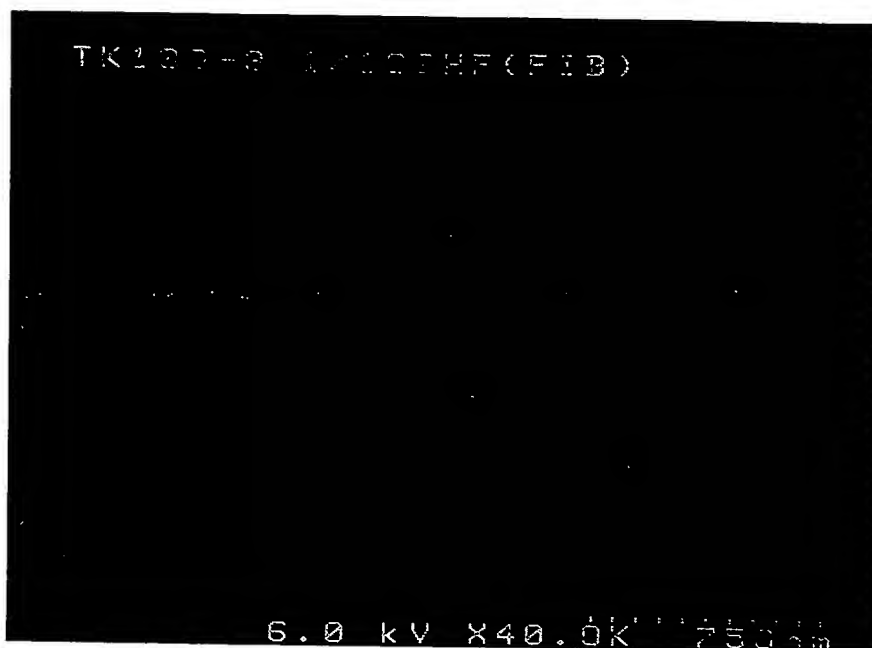


Fig. 30B

schematic diagram of enlarged electrode edge portion

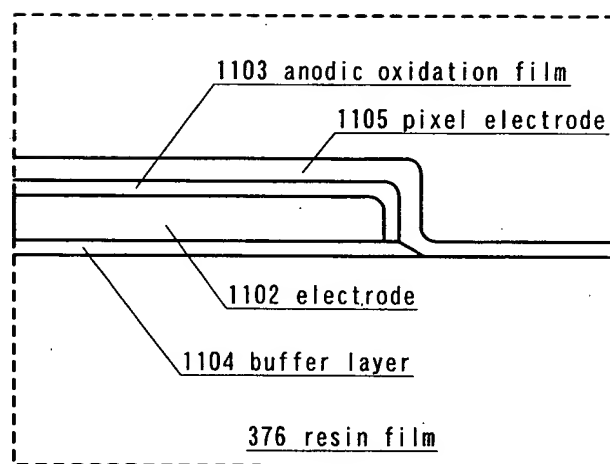


Fig. 31A

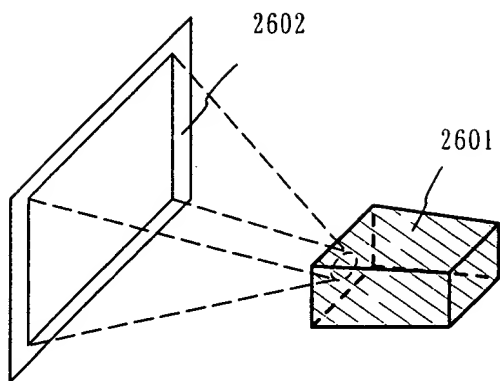


Fig. 31B

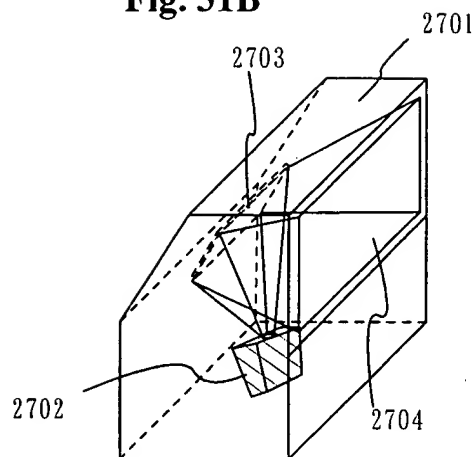


Fig. 31C projection device (three plate type)

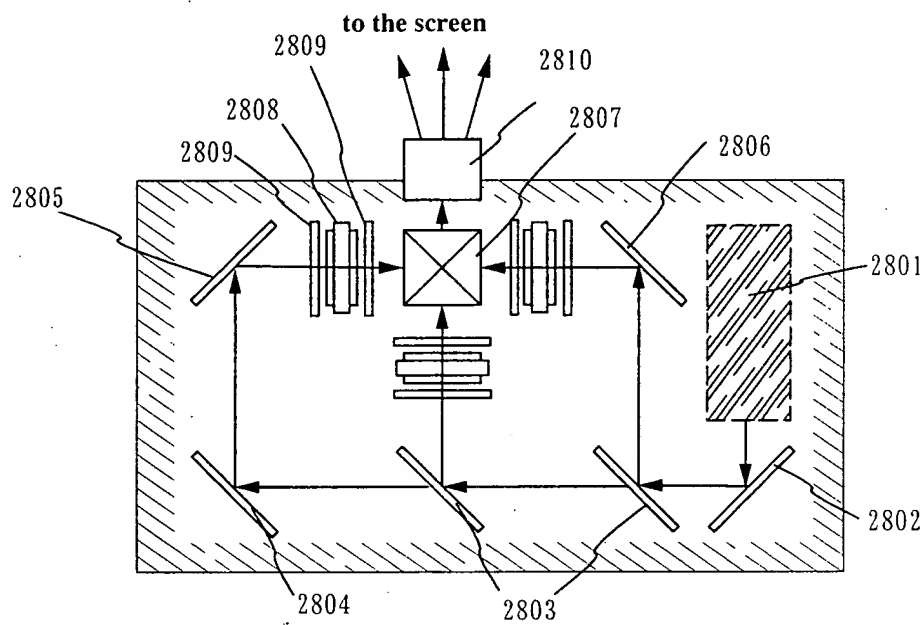


Fig. 31D optical light source system

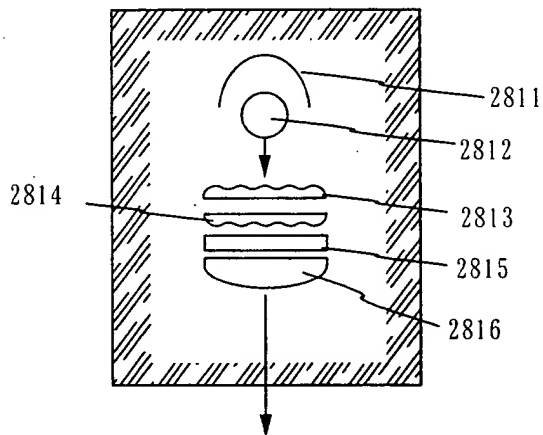


Fig. 32A

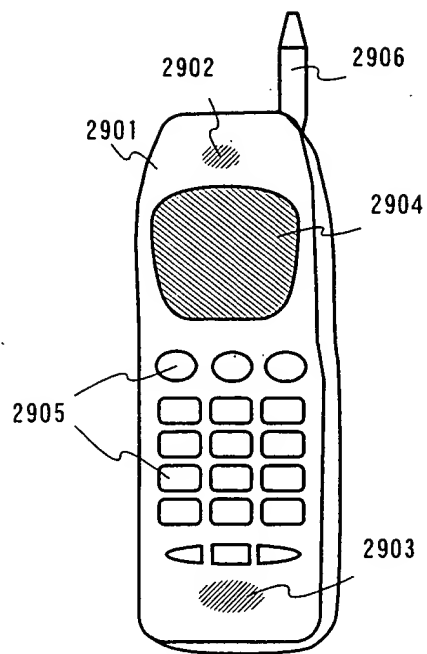


Fig. 32B

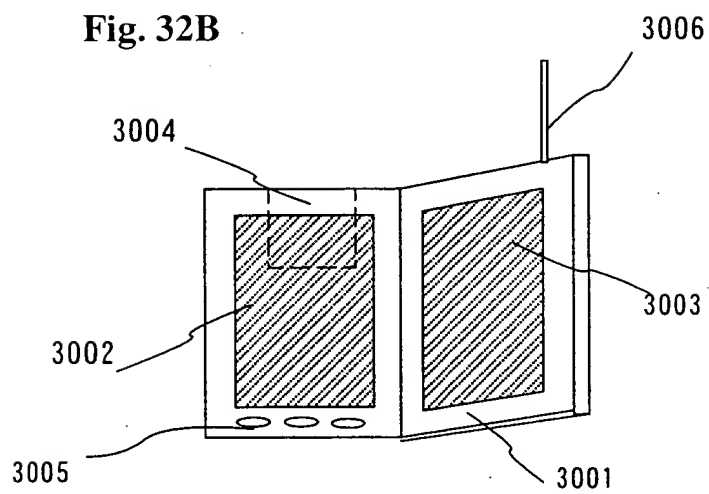


Fig. 32C

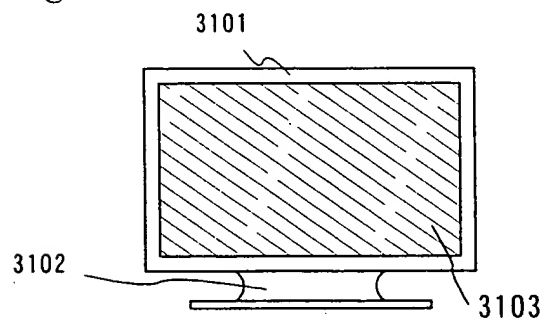


Fig. 33A

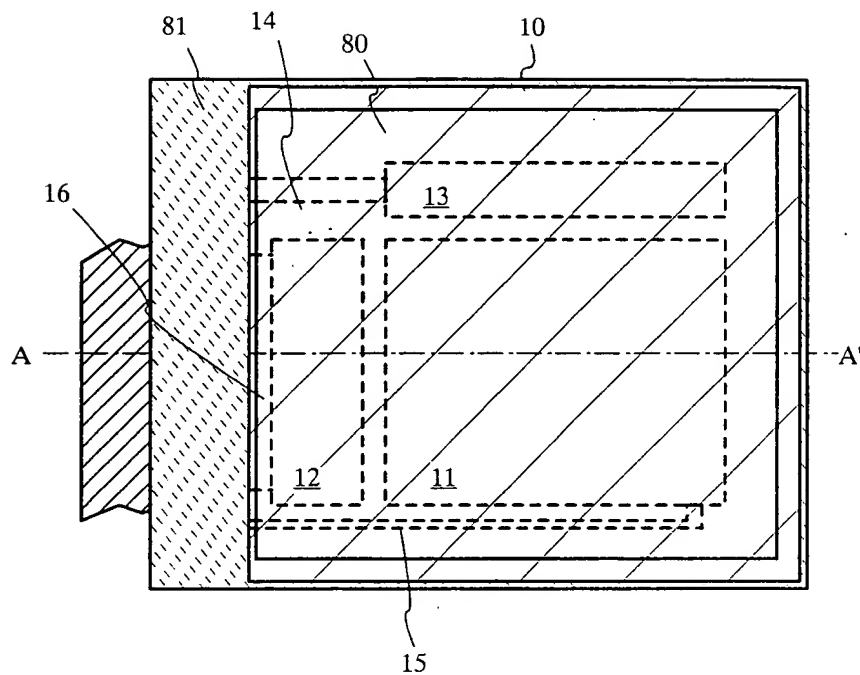


Fig. 33B

